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Empowering carbon-aware manufacturing in the semiconductor industry

g.co/hardware/CarbonAwareSemi



Google

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Photo Credit: imec

01 Introduction

Whether streaming a video, mapping driving directions, running your dishwasher, or using AI, digital life depends on semiconductors.

Semiconductor chips are the engines of computation, powering everything from everyday consumer apps to AI-driven breakthroughs in weather forecasting and drug discovery. Driven by ever-increasing global demand, the semiconductor market is on track to reach an estimated value of $1.6 trillion by 2030.

Critically, however, the semiconductor industry carries a heavy climate cost. Greenhouse gas emissions from chip manufacturing are projected to exceed 277 million metric tons of carbon dioxide equivalent (CO_2e) annually by 2030—a nearly 65% surge from 2020 levels, and roughly equal to the combined annual emissions of ten cities the size of London. As a company that designs custom chips and builds large-scale data centers, Google's carbon footprint is deeply interconnected with this industry; reducing our hardware emissions fundamentally requires decarbonizing chip manufacturing. In publishing this paper, Google is sharing pieces of a blueprint for how our industry can achieve these reductions together.



Photo Credit: imec

01 Introduction Continued...

Decarbonizing chips is particularly difficult even though emissions are concentrated within a small group of chip manufacturers. Chip designers like Google must work with chip manufacturers and suppliers to those manufacturers to validate and execute decarbonized designs. Chip manufacturing happens at an atomic scale and has long been optimized around four pillars: power, performance, area, and cost (PPAC), which do not always emphasize reducing emissions.

Coordinated decarbonization requires a shift in mindset, one where carbon footprint is actively considered during the initial conception of next-generation chip architectures and manufacturing processes. We call this carbon-aware design. This approach can be enabled by elevating environment as a fifth core metric—expanding PPAC to PPAC-E—across the design and manufacturing ecosystem. Enabling PPAC-E requires a shared understanding throughout the industry of carbon hotspots, a long-standing gap in modern chipmaking. We collaborated across the industry to help resolve this critical gap. This groundwork empowers the industry to coordinate operational interventions—including process energy efficiency, clean electricity access, and the use of gases that have a lower climate impact. Ultimately, carbon-aware design combined with lower-carbon operations becomes carbon-aware manufacturing.

Because our carbon footprints are fundamentally interconnected, every stakeholder in chipmaking has a direct incentive to help manufacturers accelerate emissions reductions. While individual companies can act independently, progress moves far faster when the industry channels its collective resources into a shared foundation. Below, we share how a set of partners including Google began building this foundation at imec (interuniversity microelectronics centre), a world-leading research hub that actively shapes the future of semiconductor process technology.

We believe that true industry transformation will occur when carbon-aware practices become embedded in the entire semiconductor industry. We hope this paper serves as a helpful step toward that end, and the body of work moves us toward more sustainable semiconductors.



Photo Credit: imec



02 Understanding the emissions landscape

Semiconductor chips are manufactured in factories known as fabs. To explore semiconductor decarbonization, we first need to understand the electricity and material requirements of a modern fab and the associated greenhouse gas emissions.

Chip manufacturing is incredibly electricity-intensive. A single fab can consume as much as 100 megawatt-hours (MWh) of electricity every single hour. Over the course of a year, a typical fab consumes as much power as approximately 80,000 U.S. homes. Over 80% of global production capacity is concentrated in Asia and often relies on fossil-fuel-heavy local grids with high carbon footprints. Some parts of the region also have limited clean electricity options. With over 80 new fabs projected to come online between 2025 and 2030, the majority of which are in this same geographical area, decarbonizing semi-conductor manufacturing electricity is a significant focus and challenge.

The materials used by the semiconductor industry present their own emission challenges. Core processes used in fabs (see "Why semiconductors are emissions intensive") are dependent on the use of fluorinated greenhouse gases (F-GHGs), some of which are directly emitted to air. F-GHGs like sulfur hexafluoride (SF_6), nitrogen trifluoride (NF_3), and carbon tetrafluoride (CF_4) are potent GHGs that can persist in the atmosphere for millennia when emitted. For example, SF_6 is 24,300 times as potent as carbon dioxide (CO_2) and persists in the atmosphere for 1,000 years. To reduce emissions, fabs use a treatment process called "abatement" to destroy greater than 90% of these gases before they are released—similar to how a catalytic converter cleans car exhaust. Even so, because their impact is so high, the small fraction of gas that escapes still has negative consequences for the climate.

Photo Credit: GlobalFoundries

The semiconductor manufacturing ecosystem

Fabs sit at the center of the semiconductor manufacturing ecosystem (Figure 1), requiring inputs of specialized silicon substrates called “wafers” alongside over 100 high-purity process gases and materials. Yet, while the inputs are diverse, the chip manufacturing process is highly consolidated: only a handful of companies operate advanced fabs, and only a few suppliers provide the equipment for each process step.[1] After the fab, the package and test stage provides the mechanical support, electrical connections, and testing required for chips to be used in data centers and devices.

While process gases, input materials, wafers, equipment, and package and test processes all generate their associated footprints, fabs account for the majority of semiconductor manufacturing emissions. Because fab emissions are heavily concentrated, we can drive significant impact by focusing on the fab through a small number of companies.

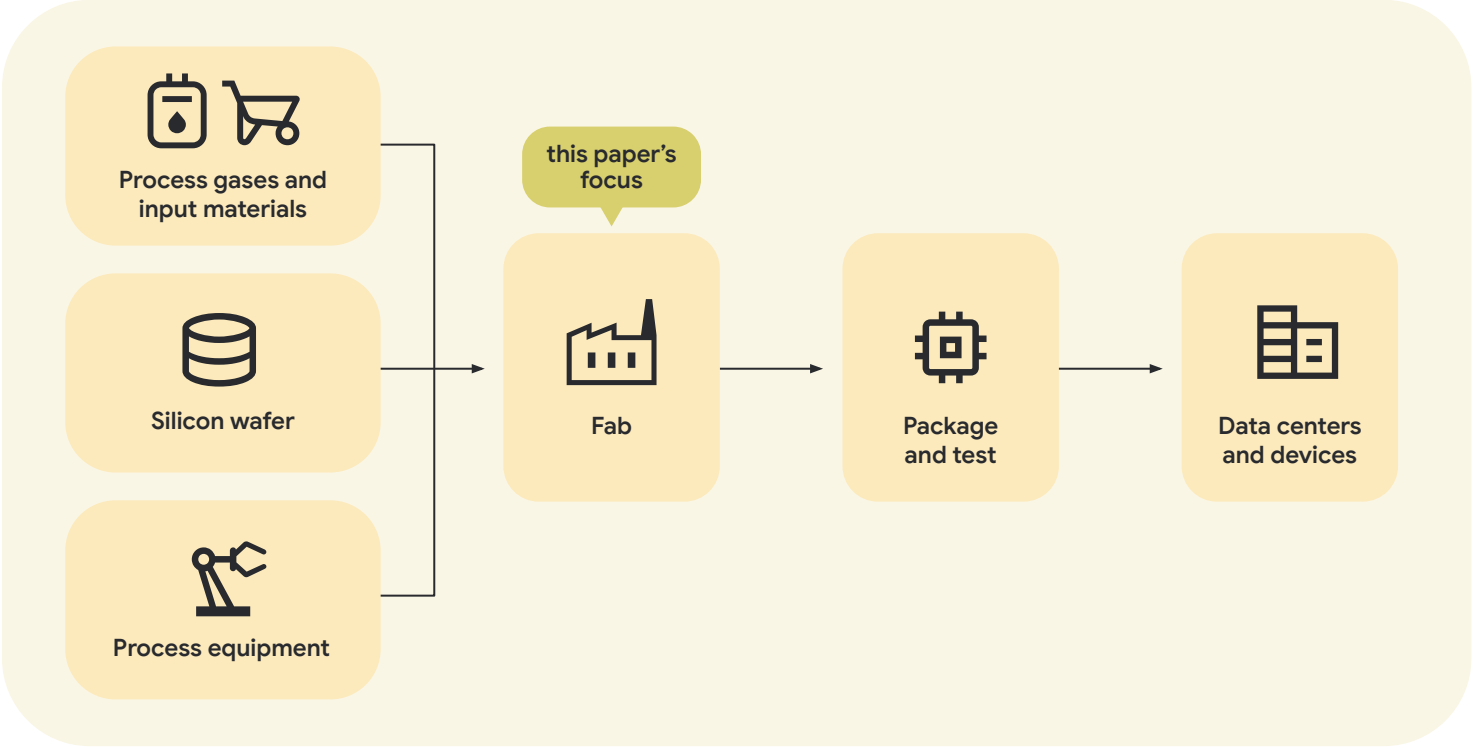


Figure 1: High-level schematic of the semiconductor manufacturing ecosystem for an advanced chip

1. Many chipmaking technologies still in use are omitted from the technical content of this paper. The total number of fabs and equipment suppliers is significantly higher.

Deep dive

Why semiconductors are emissions intensive

The foundational elements of chips are billions of microscopic electronic "switches" called transistors, connected to the outside world by equally tiny wires.

Fitting more transistors and wires into a smaller area makes a chip faster and more energy-efficient. In advanced chips, this means packing roughly 25 billion transistors that are 10,000 times thinner than a human hair into a single square centimeter.

Hundreds of chips are produced simultaneously on silicon wafers. This production process requires over 1,000 steps and takes more than three months, running continuously inside the main production environment of a fab: the cleanroom. Maintaining semiconductor cleanrooms, which are 10,000 to 100,000 times cleaner than sterile hospital operating rooms, is exceptionally electricity- and material-intensive. Below the cleanroom lies the subfab, a utility space hosting gas, chemical, and water delivery systems alongside a network of power-intensive machinery such as chillers and vacuum pumps that regulate process conditions.

Within the cleanroom, a single wafer passes through collections of lithography, etching, deposition, and cleaning tools dozens of times to create intricate three-dimensional structures layer by layer, while also undergoing repeated inspection and other processes like ion implantation and chemical-mechanical polishing. Within this repeated loop, the four core processes of lithography, etching, deposition, and cleaning detailed in Figure 2 primarily drive the chip's carbon footprint.

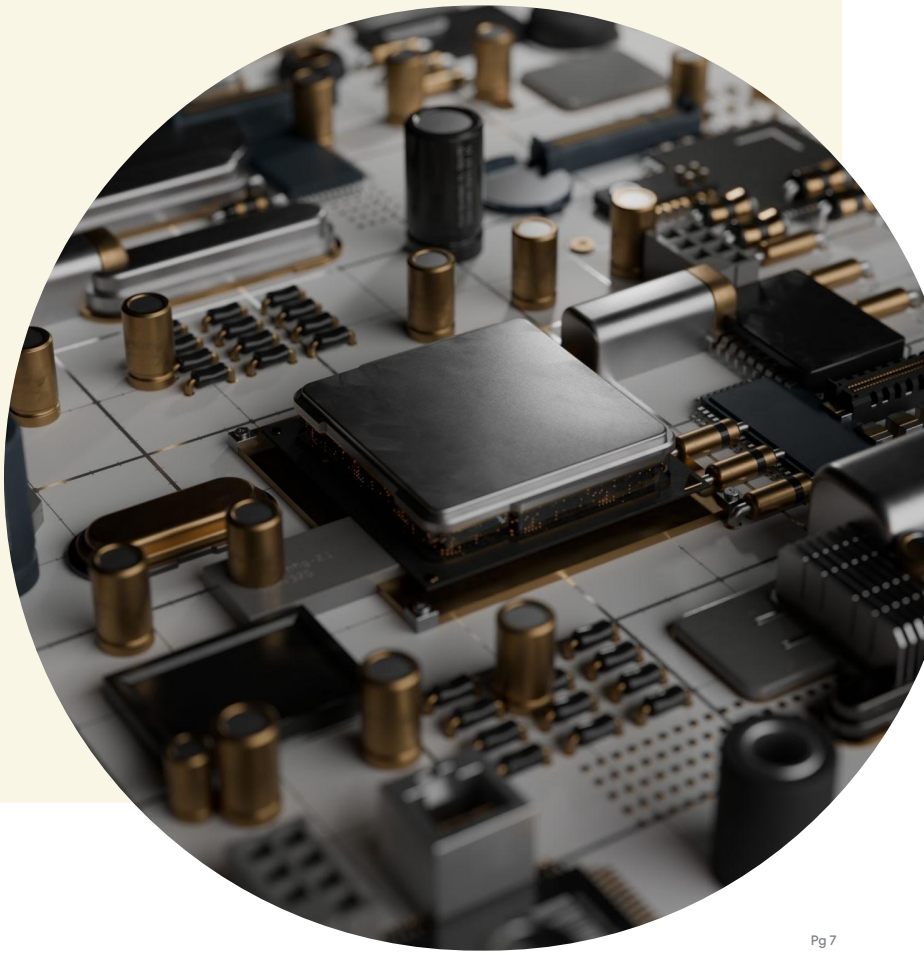


Photo Credit: MASTER, Getty Images

Deep dive

Key semiconductor fabrication process steps (simplified)

Process	Description	Fab emissions source(s)
Lithography	Printing microscopic patterns onto a chip. Lithography uses powerful lasers, precision optics, light-sensitive materials, and precise stencils to transfer an architectural blueprint onto each layer of the chip. Advanced chips can have up to 100 layers, and every single layer must line up with the one beneath it down to the nanometer. (A nanometer is about 50,000 times smaller than the width of a human hair.)	⚡
Etching	Removing targeted materials in areas defined by the lithography blueprint, using chemical reactions, to sculpt nanoscopic 3D structures. Because etching reactions rely on F-GHGs, etching is the primary source of direct emissions from a fab.	⚡ ☁
Deposition	Coating the chip with ultra-thin layers of materials that conduct or block electricity, using furnaces and plasma that consume significant electricity. Cleaning deposition chambers afterward is another chemical process that relies on F-GHGs.	⚡ ☁
Cleaning	Using sound waves, acids, bases, and ultra-pure water to wash away nanoscopic debris from wafers between steps. Because even a single speck of dust can ruin an entire chip, repeated cleaning is essential—and in total it requires a lot of electricity.	⚡

⚡ Electricity ☁ F-GHGs

Figure 2: Key semiconductor fabrication process steps and their emissions sources within the fab (simplified)

The challenge of change

Chip design is traditionally governed by four core pillars: Power, Performance, Area, and Cost (PPAC). Even minor adjustments to materials or process recipes can severely disrupt any one of them. This makes it particularly challenging to implement the desired processes and material changes necessary to decarbonize.

One way to approach these desired changes is to transition toward carbon-aware design by evolving PPAC to become PPAC-**E.** By introducing **E**nvironment as a fifth metric as early as the design stage—ideally integrated into design software—engineers could actively optimize for environmental metrics like carbon footprint with the same rigor applied to processing power or silicon area. As chip designers, Google and our peers can push for this kind of consideration.



Photo Credit: imec

However, because manufacturing is the physical source of the carbon footprint, industry-scale decarbonization requires fabs and their suppliers—along with chip designers—to embrace PPAC-E. The fab is where it all converges; fabs must embrace low-carbon innovations from their suppliers and customers (chip designers) and commit to the process development efforts required to implement them. For fab equipment manufacturers, contributing to PPAC-E could mean active consideration of the energy efficiency of their equipment operation during the equipment design stages. For process gas suppliers, it could mean greater emphasis on developing and using less potent gases.

Whole-industry PPAC-E requires a shared foundational understanding of carbon hotspots so that we neither duplicate decarbonization efforts nor leave behind carbon blind spots. Combining our backgrounds in carbon footprinting and semiconductor process engineering with our industry engagement experience, we have helped initiate and drive the foundational work needed to move toward a carbon-aware semiconductor industry.

03

Where do we start? Why footprinting matters

At Google, when it comes to carbon emissions, our approach is to focus on the larger sources first.

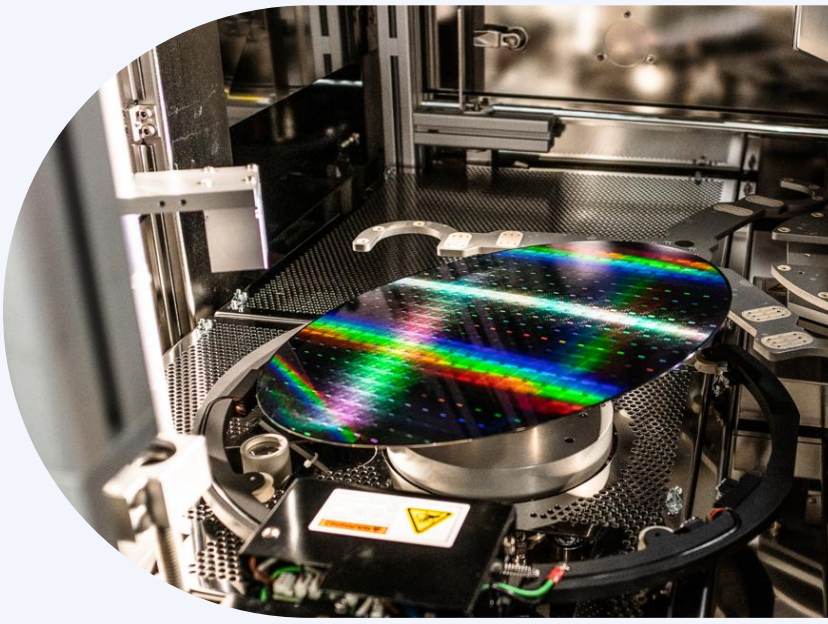
As outlined in Google's Consumer Hardware Carbon Reduction Guide, our carbon assessments rely on an iterative approach to focus on these high-impact areas. We start by using existing data to identify major carbon hotspots, then unpack those hotspots with our supply chain partners and identify specific interventions to reduce their footprint. As those emissions drop, we reassess to identify the next largest carbon driver.

Whether applying this methodology to consumer electronics or AI data centers, we see that semiconductor manufacturing is one of the most dominant manufacturing carbon hotspots. Historically, however, the industry has lacked visibility into what actually drives these semiconductor manufacturing emissions. Driven by intense market competition, semiconductor fabs have traditionally not been willing to share specific data relevant to the carbon footprint of the chips with Google and other customers.

Given that, if fabs are proprietary, how did we know semiconductors were a carbon hotspot?

We started with the best data available at the time. For many years, the industry relied on emissions models established around 2011. At that time, chips were manufactured using flat, two-dimensional (2D) transistor architectures.[2] For over a decade, this "2D model" was perfectly acceptable for identifying hotspots in chip manufacturing.

However, by the late 2010s, chip manufacturing became substantially more complex, and the 2D model was no longer representative of the most advanced chipmaking.



2. While transistors form a chip's foundation, transforming them into a functional circuit requires stacking many layers to route signals and interface with the outside world. Even chips built with 2D transistors rely on multi-layered structures.

Photo Credit: imec

The divergence

As fabs evolved and transformed their manufacturing processes to make chips more powerful, faster, and more efficient, they could no longer squeeze more transistors onto a flat surface.

To achieve the desired transistor density, they had to start building upward, entering the "3D" era around 2014. (Think of the architectural differences in a rural area, where buildings are typically shorter and more spread out, vs a dense urban city, where skyscrapers are prevalent.)

We are now entering a period where 3D transistors are stacked upon one another (Figure 3). 3D transistors, substantially denser wiring, and other material innovations require even more intensive manufacturing processes than 2D chips.

3D architectures rely on **lithography lasers ten times more powerful** than previously used and more F-GHG-based etching processes. These processes consume more electricity and produce more direct emissions than the 2D transistors that were commonplace in 2011.

By the late 2010s, it became clear that using 2D models to estimate the carbon footprint of 3D architecture would underestimate the real carbon footprint of modern semiconductors, distorting our understanding of process hotspots and thus any strategies we might design to decarbonize the sector efficiently.

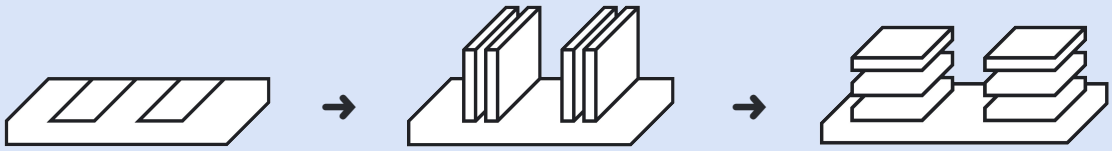


Figure 3: Evolution of the geometry of transistors in logic[3] chips (figure courtesy of imec)

3. For simplicity, our analysis focuses on logic chips that process data, but the conclusions also apply to memory chips that store data.

04

How do we focus?

The Sustainable Semiconductor Technologies & Systems (SSTS) community

Without a carbon model that reflected the reality of 3D architecture, the industry couldn't effectively focus its decarbonization efforts, to say nothing of collaborating on carbon-aware design.

However, as we sought to build an updated baseline, we recognized that expecting fabs to provide detailed process information overlooks why they function in such a proprietary fashion in the first place: protecting advanced process methodologies is essential for fabs.

This created a challenging obstacle: how do we acquire the foundational data needed to advance carbon-awareness for chips without access to data from the fabs?

"The shift in chip architectures opened the door to reimagine the industry's carbon footprinting foundation. As an institution that actively shapes the future of semiconductor manufacturing, imec was the perfect partner."

— Joe

Decarbonization and Environmental Footprinting Lead, Platforms & Devices



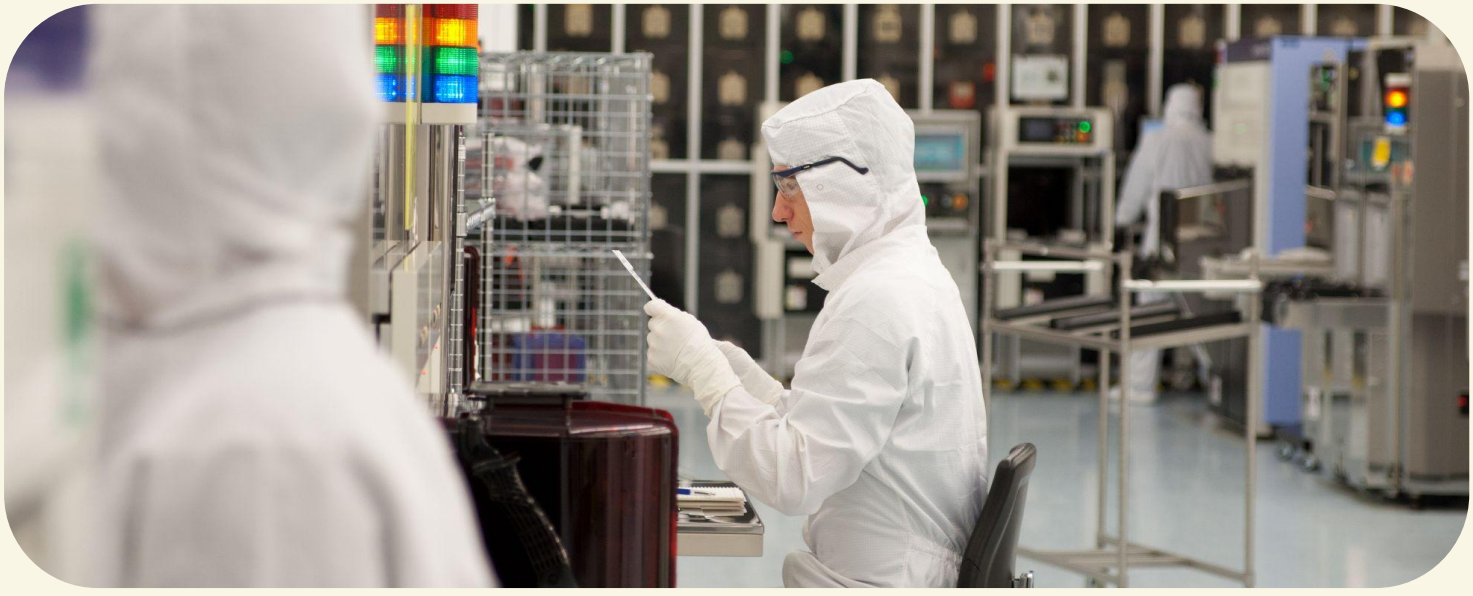


Photo Credit: imec



Photo Credit: imec

The inception of SSTS

To overcome this obstacle, we engaged with imec—a well-respected and established nonprofit semiconductor research organization. Imec was uniquely positioned to help because it operates its own state-of-the-art R&D fab equipped with the most advanced process equipment used by commercial fabs. Unlike commercial fabs, imec operates using a collaborative, self-governing program model that emphasizes data transparency. We realized we could use imec's facility to both gather real emissions data on advanced processes and conduct R&D to decarbonize them.

Thus, a group of companies including Google came together in 2021 to support the creation of the **Sustainable Semiconductor Technologies & Systems** (SSTS) program.

Since its inception, SSTS has evolved into a community of partners spanning the semiconductor ecosystem including:

- Data Centers & Devices
- Fabs
- Equipment Suppliers
- Material Suppliers
- Design Software

Building a “virtual fab”

We needed to create a new emissions baseline. With this, we could gain insights into where to focus decarbonization R&D at imec. The SSTS team collected data on the energy and materials consumed, as well as the emissions generated by the equipment in imec’s fab, leading to the creation of **imec.netzero (iNZ)**—a first-of-its-kind “virtual fab.”

iNZ provides transparency into the carbon footprint of chips process by process, enabling us to better focus fab decarbonization efforts as an industry (Figure 4). A basic version of iNZ is also publicly available, giving researchers, policymakers, and the public greater visibility into the carbon footprint of modern chip technologies.

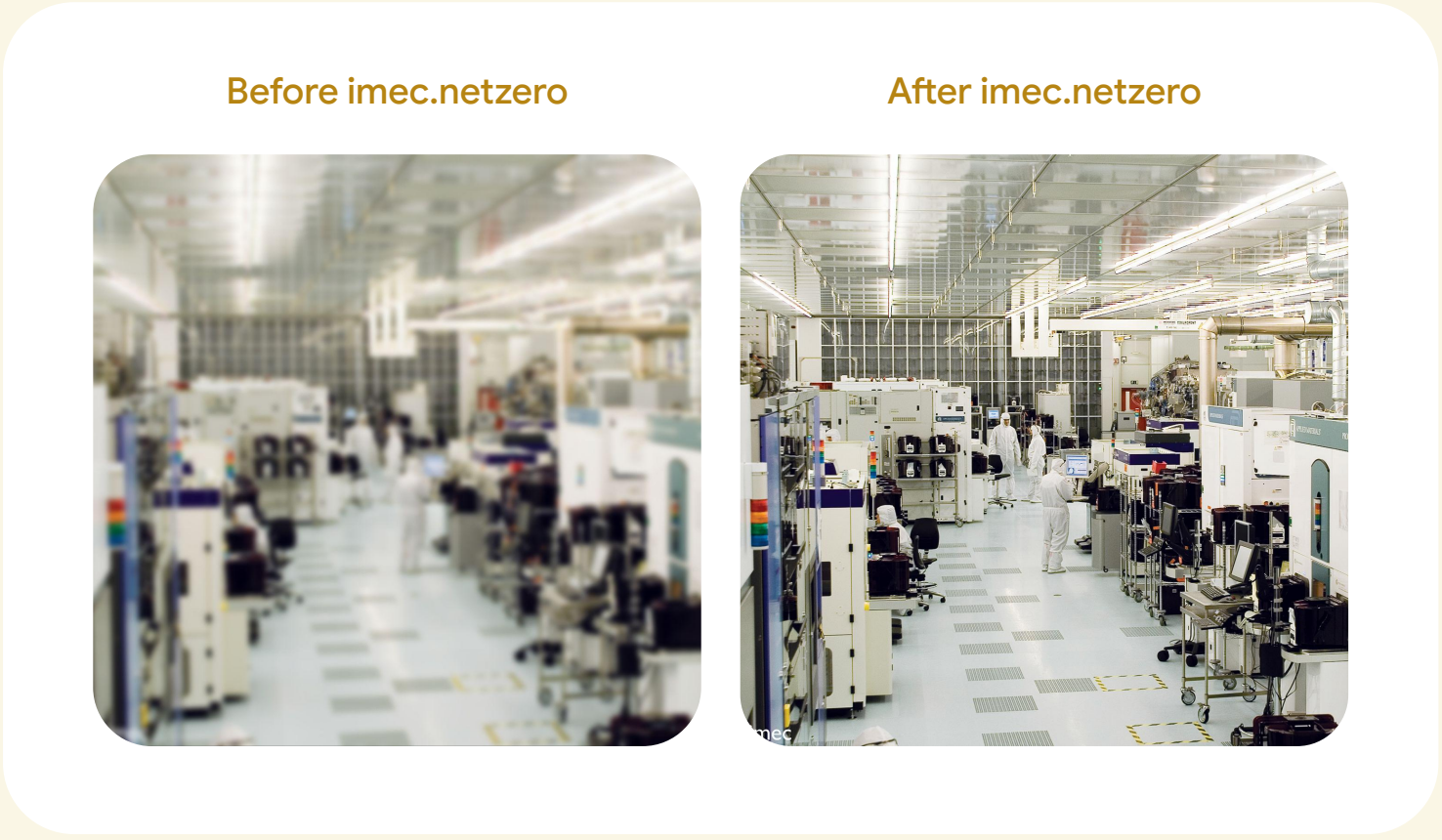


Figure 4: imec.netzero brings the chipmaking process into focus in the context of carbon footprint.

Photo Credit: imec

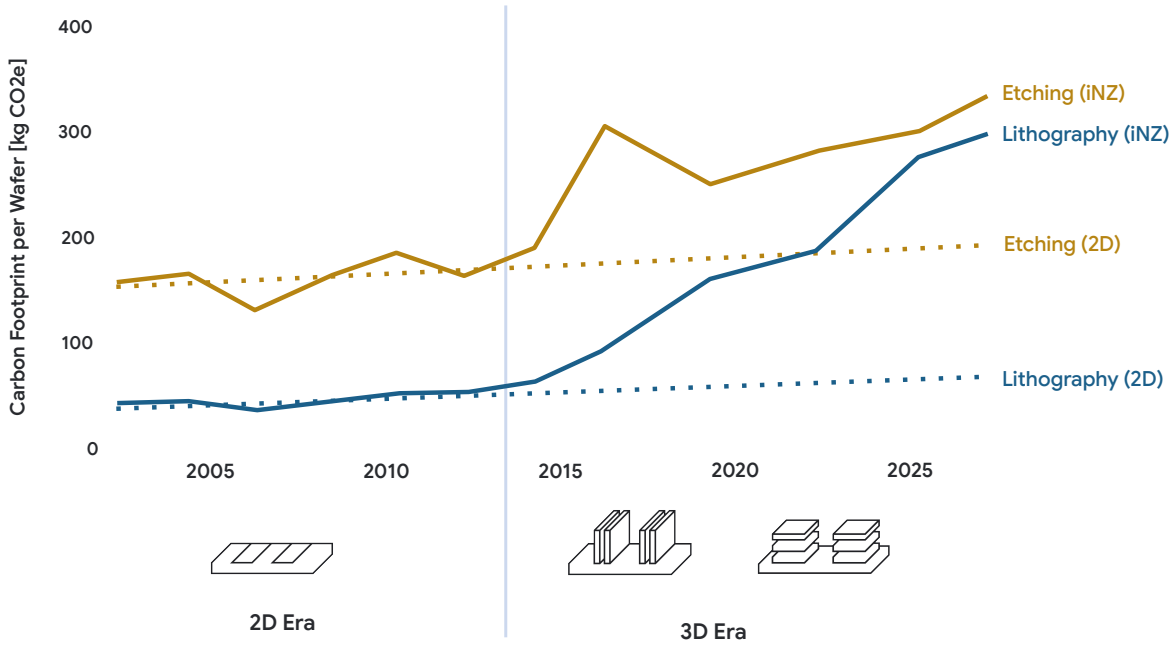


Figure 5: Process-level carbon footprints of advanced logic semiconductors across technology mass-production launch years. Structural transitions to 3D etching and higher-power lithography surpassed what could be captured by 2D carbon models, leading to the need to create a new model.

. . . .

Dashed lines:
Extrapolated trends projecting 2D-era etching and lithography carbon footprints into the 3D era.

Solid lines:
Updated carbon footprint estimates from iNZ.

Underlying data generated using imec.netzero v7.0.0 in July 2026

imec.netzero quickly confirmed that the carbon footprints of etching and lithography in the 3D era diverge dramatically from an extrapolation of 2D chipmaking (Figure 5).

Google has already adopted imec.netzero for our carbon footprinting in internal and public reporting, including for our consumer devices since mid-2024. This enables prioritization of decarbonization for the latest logic technologies (Deep dive: Learning in action—decarbonizing today's chips). Decarbonizing at the industry level is a group effort, and we need universal participation.

Google encourages the entire semiconductor industry to adopt and help refine imec.netzero for semiconductor carbon footprinting.

Deep dive

Learning in action: Decarbonizing today's chips

To demonstrate imec.netzero in practice, we use it to establish a carbon hotspot baseline for logic chips launched in the 2026-2027 timeframe, examining only direct fab operation and the upstream supply chain (package and test, chip use, and end-of-life are excluded).

We start by assuming zero sustainability interventions, thus excluding F-GHG abatement and any clean electricity beyond an average manufacturing grid. While this worst-case scenario rarely reflects reality, it serves as an easy-to-understand starting point to evaluate the impact of specific decarbonization efforts.

We split emissions by category: direct fab emissions, electricity generation, and the upstream supply chain. We then map each of these categories by process type, creating a comprehensive emission-by-process heatmap. The data shows that, without interventions, direct process emissions from etching would be the chip's primary carbon hotspot, while deposition and lithography dominate electricity consumption (Figure S1). By assessing these contributions this way, we can determine which decarbonization interventions deliver the maximum impact and should thus be our first priorities.

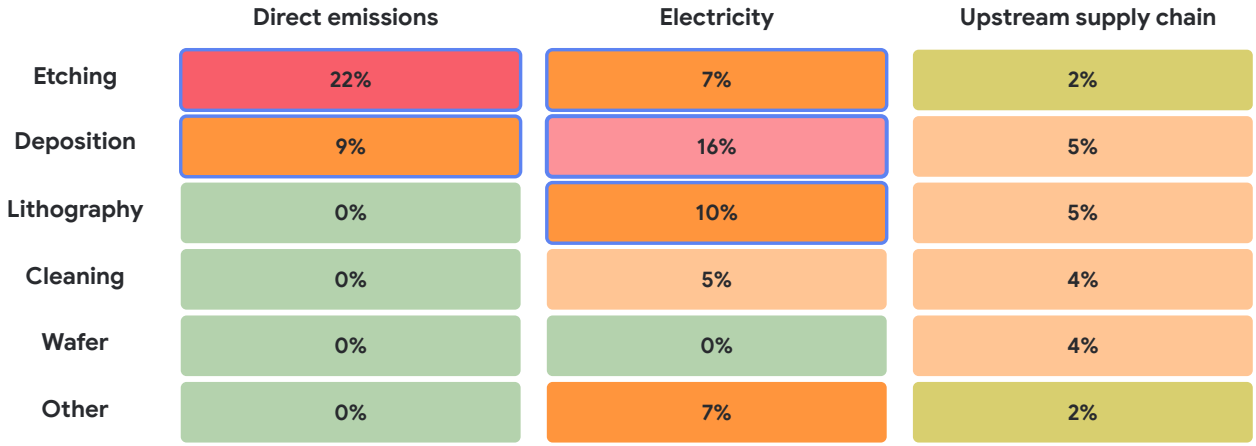


Figure S1: The impact of direct emissions from etching and deposition, along with the impact of electricity for etching, deposition, and lithography contributes nearly 65% of the total impact of the chip, before any interventions. The top five hotspots are outlined in blue.

Underlying data generated using imec.netzero v7.0.0 in July 2026

Deep dive

Learning in action: Decarbonizing today's chips

In practice, real-world fabs use abatement systems to reduce F-GHG (direct) emissions from process gases. These systems typically combust exhaust gases from process equipment and then treat or "scrub" them before release. Their effectiveness is measured by Destruction and Removal Efficiency (DRE), which quantifies the reduction in greenhouse gas potency between entering the process and being emitted into the air. Abatement is widely deployed across the industry, and so we apply a DRE of 90% to our model, after which the majority of the chip's carbon footprint is from fab electricity (Figure S2). This is a more representative baseline of real-world emissions.

Clean electricity for the fab is the single biggest decarbonization lever we have for semiconductors (even without abatement!). Clean electricity is widely available in some regions (particularly North America and Europe) and is less widely available in many regions in Asia, including where most of the fabs are located. Google is working across the industry to navigate clean electricity supply challenges and increase clean electricity access in critical areas like Taiwan, South Korea, and Japan. We partnered with BlackRock and local developers to build and deploy clean electricity in Taiwan and make some of it available for our supply chain. In Japan, we helped retrofit a hydropower plant to enable clean electricity use by part of our supply chain. And we continue to pursue market reform advocacy and training that supports clean electricity procurement and mobilization.

While both F-GHG abatement and clean electricity are crucial avenues for chip decarbonization, they mostly operate independently of the underlying fab processes themselves. Achieving even deeper decarbonization requires us to address carbon before it is emitted—directly at the process level. Because coordinated research of this kind has historically been missing across the industry, a core focus of imec SSTS is to leverage imec's state-of-the-art facility to facilitate lower-carbon process development, as described in Section 05.

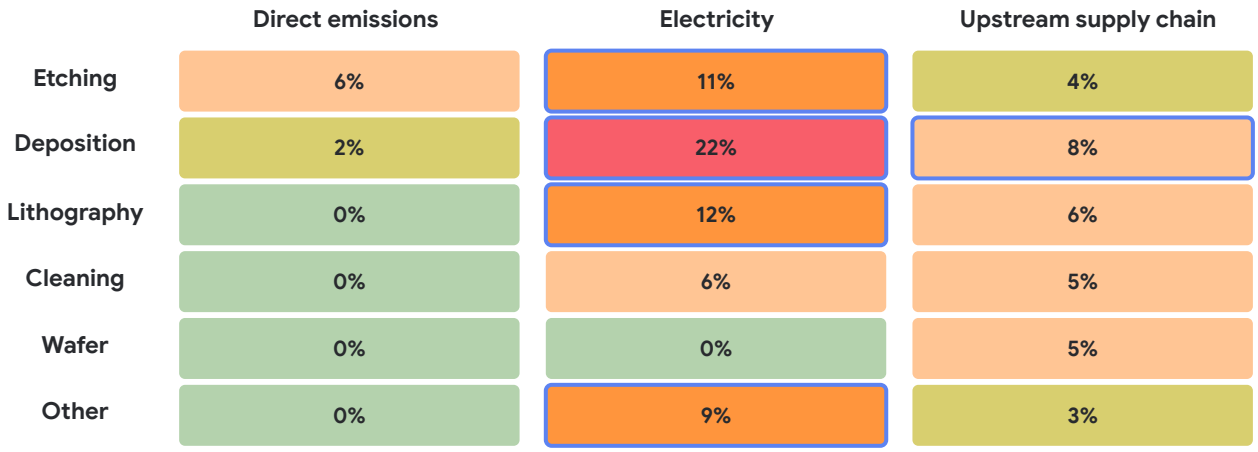
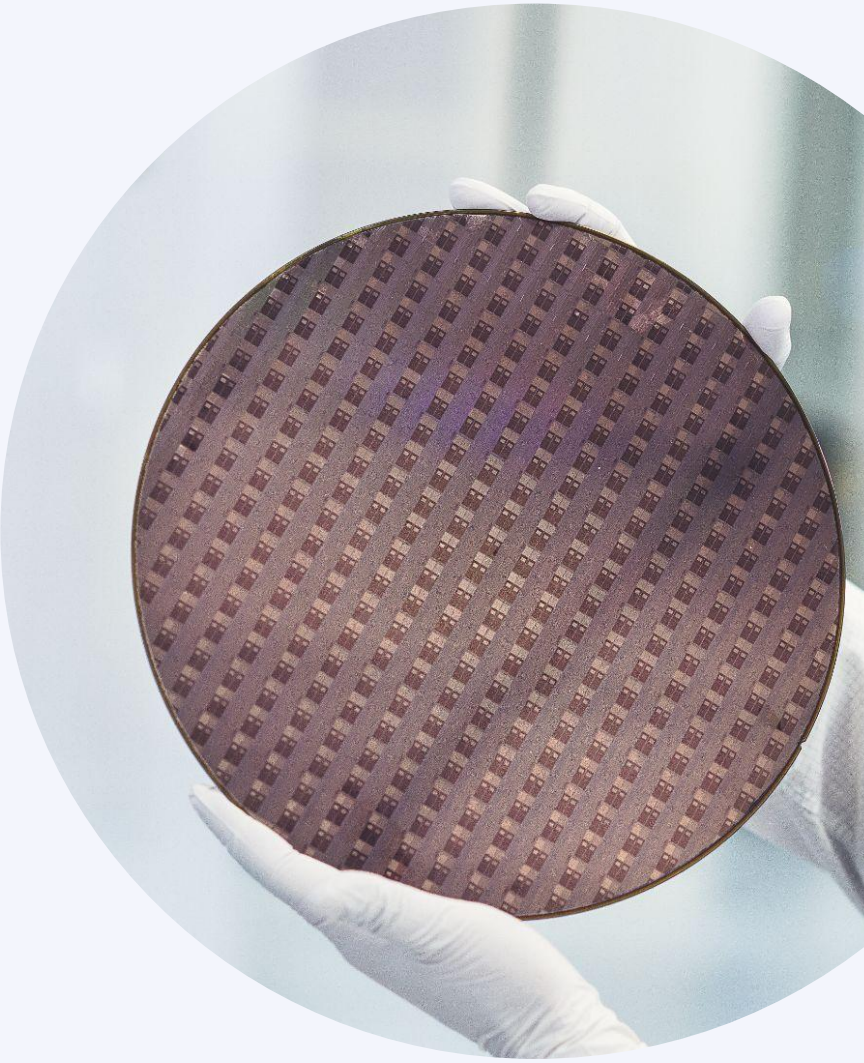


Figure S2: Hotspot map after applying in-fab abatement with 90% DRE, a realistic baseline for current manufacturing practices. The top five hotspots are outlined in blue.

Underlying data generated using imec.netzero v7.0.0 in July 2026

05

Turning data into change



Advancing data

The imec.netzero platform empowers the semiconductor industry with a common understanding of carbon hotspots and the ability to collaborate on carbon-aware semiconductor manufacturing. Because of our deeply interconnected footprints, adoption of imec.netzero for carbon footprinting across the entire industry is essential to prevent fragmented accounting and align shared climate goals. To drive consensus on this, we are advocating through Semiconductor Equipment & Materials International (SEMI) for imec.netzero to serve as the common decarbonization baseline for over 200 ecosystem members, and through the Open Compute Project (OCP) to establish imec.netzero as the emissions accounting basis for chips and advanced electronic packages used in data center hardware.

In 2024, Google co-led a SEMI working group to address fab "data request fatigue" caused by fragmented carbon footprint surveys from Google and its peers. Imec.netzero resolved much of this challenge by providing a first-of-a-kind baseline that dramatically reduces the data needed to determine a modern chip's carbon footprint. However, tailoring carbon estimates to a specific chip still requires a few real-world data points from fabs. Imec.netzero helped the SEMI working group pinpoint a concise set of critical inputs.

Our common data request is now shaping the development of broader best-practice guidelines for semiconductor carbon footprinting.
To ensure maximum impact, we strongly support open-sourcing data request templates and forthcoming best-practice recommendations.

Aligning the industry on data, however, is only the beginning. With a shared hotspot map established, the next challenge is to develop and test new processes and materials to reduce the impact of those hotspots.

Photo Credit: imec

Advancing change

Imec operates on a collaborative model built around partner participation in a diverse array of cross-industry programs including SSTS. To support this, imec provides a pre-competitive environment where partners can test new materials and equipment, and develop new processes. Within this framework, SSTS leverages imec's leading-edge facilities and equipment to conduct specific research and development, focusing directly on the emission hotspots identified by imec.netzero.



Photo Credit: imec

For example, to tackle the long-term challenge of replacing high-potency GHGs in etching processes with lower-potency alternative gases, imec launched a project, with Google's support, that focuses on testing promising alternative gases on leading-edge etching equipment. Using industry-scale etching equipment hosted at their facility, imec will generate transparent process performance data for alternative gases under manufacturing-relevant conditions—enabling the SSTS community to evaluate viable alternative gases together and de-risk their introduction to manufacturing. Imec is also investigating energy efficiency in lithography, one of chip manufacturing's most power-intensive steps. Emerging lithography materials and process conditions can reduce the total electricity required to expose wafers to laser light during this step. This also has the potential to increase wafer throughput and reduce overall fab electricity consumption.

However, process-level R&D is only effective if we engage the broader ecosystem to translate successful breakthroughs into widely adopted, lower-carbon processes. Just as with imec.netzero on the data and modeling side, Google works with SEMI to encourage participation in pre-competitive decarbonization efforts across the wider community. For instance, discussions at the SEMI Global Executive Summit in 2025 convened industry executives spanning chemical suppliers, equipment manufacturers, and fabs to align on the critical value of shared testing platforms including those at imec, and more.

While imec offers a leading blueprint for this work, no single company or institution can solve these manufacturing challenges alone. We invite research institutions and industry partners worldwide to support collaborative platforms that help address emissions hotspots in the semiconductor industry.



Photo Credit: GlobalFoundries

06 Future horizons

Collaboration

Our ultimate goal is to align the semiconductor ecosystem on a collaborative decarbonization framework, anchored in transparent data models and R&D platforms. Through SSTS, the industry has established modern emissions baselines grounded in current manufacturing realities that allow chip designers, equipment makers, and fabs to address carbon hotspots using a common carbon hotspot understanding.

However, a shared understanding alone cannot decarbonize a fab; we must also collaborate on R&D to validate new solutions without the risk of disrupting active production lines. By sharing data **and** testing across the supply chain, we create the confidence to deploy lower-carbon processes and materials into high-volume production.

Early engagement

The most efficient way to eliminate carbon is to never emit it in the first place. The long-term ambition of a PPAC-E framework is to bring carbon-awareness directly to the silicon engineer's desk and into fab operations. By integrating imec.netzero data directly into chip design software, for example, silicon engineers could evaluate the real-time carbon impact of design choices like layer stacking or transistor geometry. This early visibility turns emissions into an actionable design variable—one that can be weighed against power, performance, area, and cost. While full business considerations are more complicated than simply having the data, integrating carbon information enables its consideration at the earliest phases.



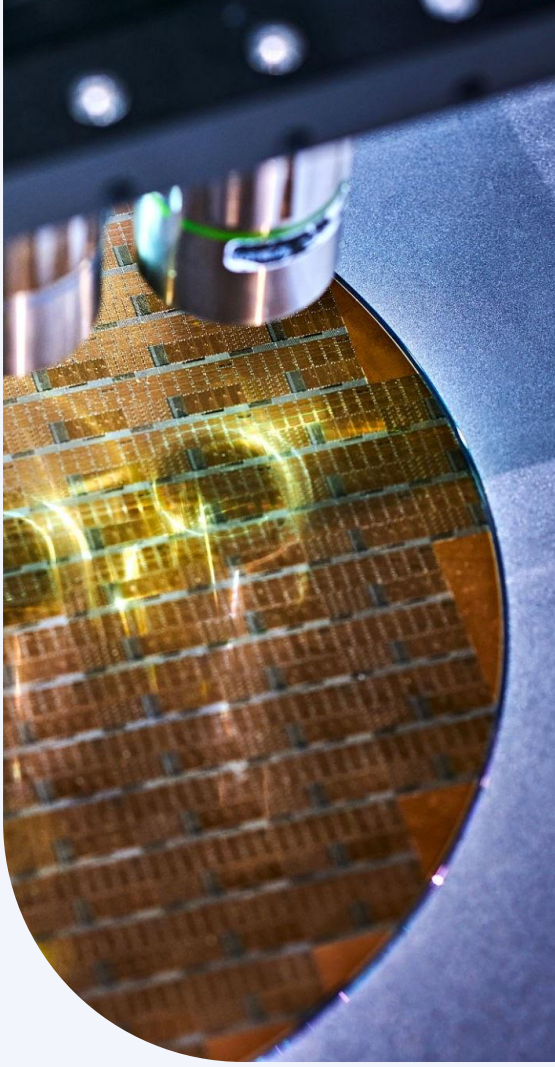
Photo Credit: zorazhuang, Getty Images

Broader sustainability

A comprehensive approach to sustainability requires looking beyond carbon footprint alone. To prevent unintended tradeoffs from decarbonization, Google strongly supports imec's ongoing efforts to consider an expanded set of environmental impacts within SSTS.

Partners can pilot sustainability-driven R&D across four focus areas including traditional decarbonization topics such as energy efficiency and greenhouse gas mitigation, and also water management and material circularity. Future versions of imec.netzero will incorporate data on water use, circularity, and human toxicity, among others.

We can also broaden our impact by taking a wider view in time—one that goes beyond initial production and into the hands of the people using devices. Deeper insight into semiconductors' manufacturing footprint also informs our users. For example, when users keep their devices active for longer, they get more out of the materials and energy already invested in those chips and may reduce the need for new production. Communicating the environmental savings of extending a device's life requires the accurate baseline impact metrics that this work is enabling.



07
Conclusion

As we have explored, while chips are at the center of our modern digital lives, their manufacturing carries a climate cost driven by fabs that are electricity-intensive and emit potent greenhouse gases.

For years, outdated emissions models based on 2D chipmaking created a significant blind spot in carbon-awareness because chip architectures had moved into more carbon-intensive 3D realms. By convening partners across the semiconductor industry around a shared carbon framework, we began bridging this gap. Establishing a transparent data foundation through imec's SSTS program and virtual fab brought modern carbon hotspots into sharp focus. Now, we are advocating for using the virtual fab as a basis for the industry to consider the environment alongside the traditional metrics of power, performance, area, and cost. We see this as crucial groundwork for a future semiconductor industry to truly embrace carbon-aware design.

Empowering a carbon-aware semiconductor industry through SSTS underscores the vital role of pre-competitive collaboration. Using trusted models—portions of which are open to the public—and a consensus on hotspots, SSTS proves that a complex industry can unite around a shared carbon footprint understanding. While coordinated decarbonization remains a long-term goal, this marks a promising starting point. We invite the semiconductor industry and other industries alike to join the conversation: what do you think of this approach, and how can we build on it together?

Photo Credit: Comezora, Getty Images

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We also thank our collaborators for their contributions to the paper and the work behind it:

Aditi Kale, Anna Meegan, Cedric Rolin, David Bourne, Emily Gallagher, Kevin Martins, Lars-Åke Ragnarsson, and Mike Labanowski

Resources and references

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